General Description

The APT JGGÍÓ is a high efficiency current-mode boost converter with a fixed operation frequency. The PT JGGÍÓ has been integrated a very low Rds-on NMOSFET to reduce power loss and achieve high efficiency. The maximum efficiency is up to 93%. The output Voltage can be programmed by feedback resistances, and the maximum output voltage is 10V. PT JGGÍÓ can output 2A current when VIN is higher than 3.3V and output is 5V. 1.2MHz operation frequency minimizes L and C value, and internal compensation network reduces external component counts. ESOP-8 package provides the best solution for PCBheat dissipation.

Features

· Wide Input Range: 2.F-6V Input,·

· PT JGGÍÓ Up To 2A Output Current

· 1.2MHz Switching Frequency

· Low RDS(ON): 70mΩ

· Up to 93% Efficiency

. Over Voltage Protection

· Under-Voltage Lockout Protection

· Over-Temperature Protection

· Internal Soft Start

· 1uA Shutdown Current

· Accurate Reference: 0.6V VREF

· Compact package: ESOP-8

Pin Configuration

Applications

TOP VIEW

NC	1			8	NC
GND	2	Thermal Pad GND		7	SW
VIN	3			6	FB
EN	4			5	NC

SOP8-EP
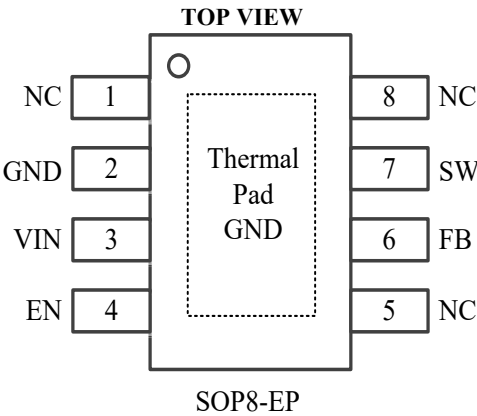
Pin Descriptions

Pin Name	Symbol	Pin Function
1	NC	No connection
2	GND	GND
3	VIN	Input supply pin. Must be locally bypassed.
4	EN	Enable pin. A high input at EN enables the device and a low input disables the devices.
5	NC	No connection
6	FB	Feedback
7	SW	Power switch output. Connect the inductor and the blocking Schottky diode to SW.
8	NC	No connection
9	Thermal Pad	GND

■ **Block Diagram**

J O ; 447D
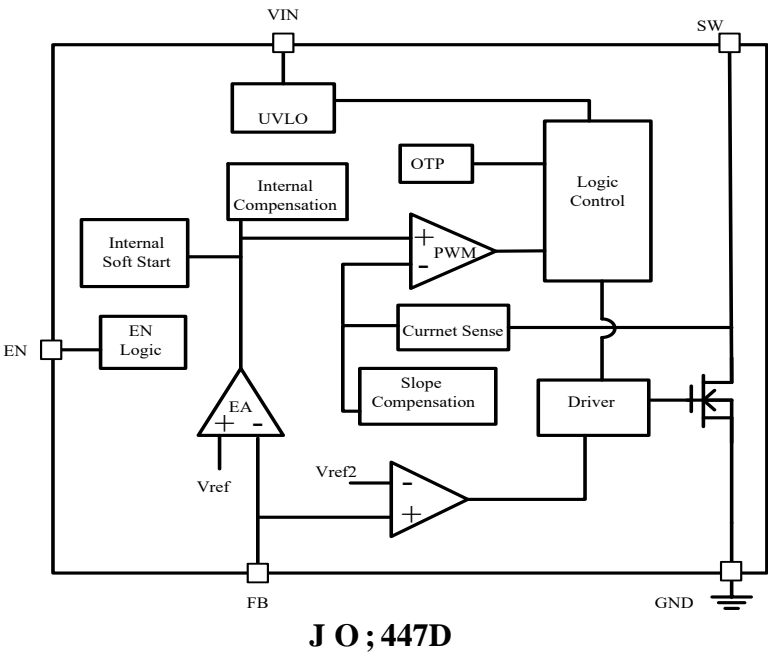
■ **Absolute Maximum Ratings**

SYMBOL	NAME	VALUE	UNIT
V_{IN}	Input Voltage	-0.3～6.5	V
V_{SW}	Voltage at SW Pin	-0.5～12	V
V_{IO}	All Other I/O Pins	GND-0.3 to VDD+0.3	V
P_{TR1}	Thermal Resistance(SOT23-6) Θ_{JA}	40	℃/W
T_{stg}	Storage Temperature	-55 to 150	℃
T_{solder}	Package Lead Soldering Temperature	260℃, 10s	
ESD Susceptibility	HBM(Human Body Mode)	2	kV

Note1: Exceeding these ratings may damage the device.

■ **Recommended Operating Conditions(Note 2)**

SYMBOL	NAME	VALUE	UNIT
V_{IN}	VIN Supply Voltage	2.F to +6	V
V_{SW}	Output Voltage	$V_{IN}$to 10	V
T_{OTP}	Operating Temperature	-40 to +85	℃

Note2: The device is not guaranteed to function outside of its operating rating.

■ Electrical Characteristics

(VIN = 3.3V, VOUT=5V, IOUT=100mA, TA = 25°C unless otherwise specified)

SYMBOL	ITEMS	CONDITIONS	Min.	Typ.	Max.	UNIT
V_{IN}	Input Voltage		2.1		6	V
Feedback						
V_{FB}	Feedback Voltage		588	600	612	mV
I_{bias}	FB Pin Input Bias Current			0.05	1	µA
UVLO						
UVLO	Under Voltage Lock Out			2.1		V
Operating Current						
I_{off}	Operating Current（Shutdown）	Vout disconnected with schottky		0.1	1	µA
I_{sby}	No Switching	Vin=3V VFB=0.7V		100		µA
F_{sw}	Switching Frequency			1.2		MHz
D_{max}	Maximum Duty Cycle	V_{FB}=0V		90		%
Chip Enable						
V_{EN_H}	EN Minimum High Level		1.5			V
V_{EN_L}	EN Maximum Low Level				0.4	V
V_{HYS}	EN Hysteresis			90		mV
I_{EN}	EN Input Bias Current				1	µA
OTP						
OTP				160		°C
OTP Hystersis				20		°C
Output Switch						
R_{ON}	SW On Resistance (Note 3)			70		mΩ
I_{PEAK}				4.5		A
I_{LEAK}	SW Leakage Current	V_{sw}＝5V		0.01	1	µA
Open Circuit Protection						
	ÁPT JGGÍ Ó///////////////////////////////X$_{OUT}$			V_{OUT}×112%		V
Soft Start						
t_{ss}	Soft Start Time (Note 3)	V_{IN} Power On		400		µS

Note3: Guaranteed by design.

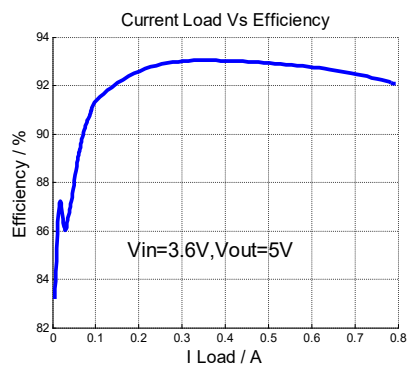## ■ Typical Performance Characteristics
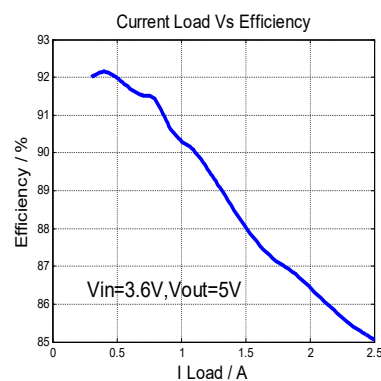

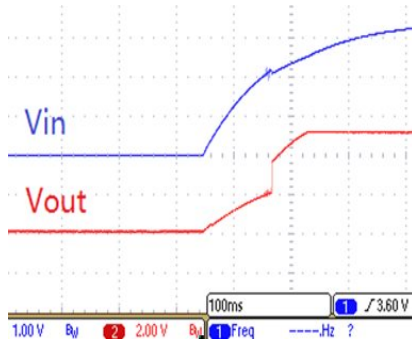Fig 1 Efficiency Vs Light Load

Fig 2 Efficiency Vs Heavy Load
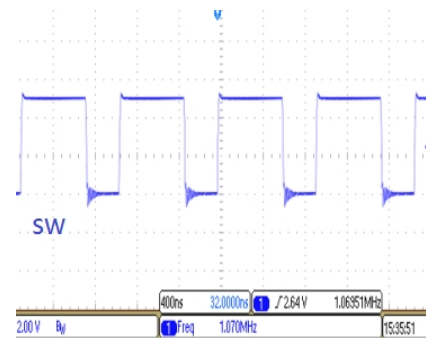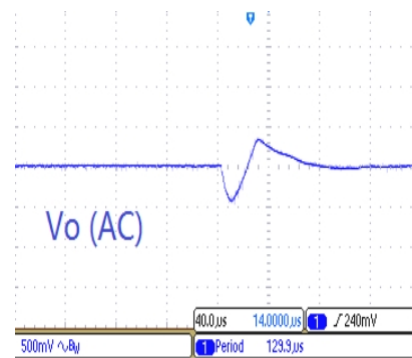
Fig 3 Startup with V_{in}

Fig 4 SW Waveform

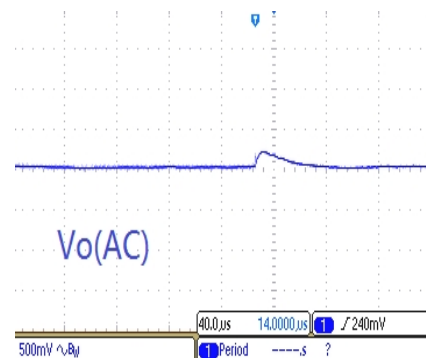Fig 5 Transient Response
(V_{IN}=3.6V, Vout=5V, I_{load}=0.15A to 0.9A)

Fig 6 Transient Response
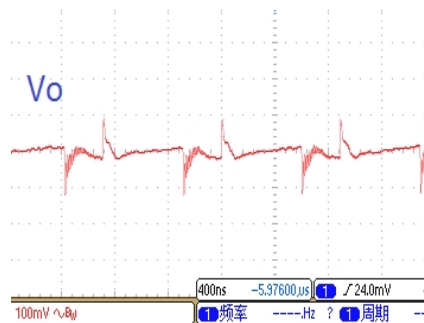(V_{IN}=3.6V, Vout=5V, I_{load}=0.9A to 0.15A)
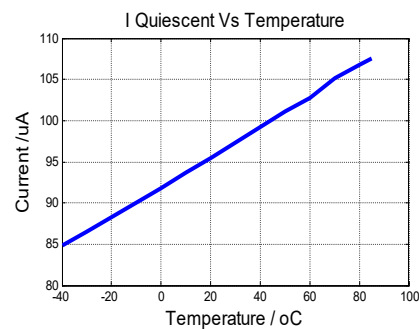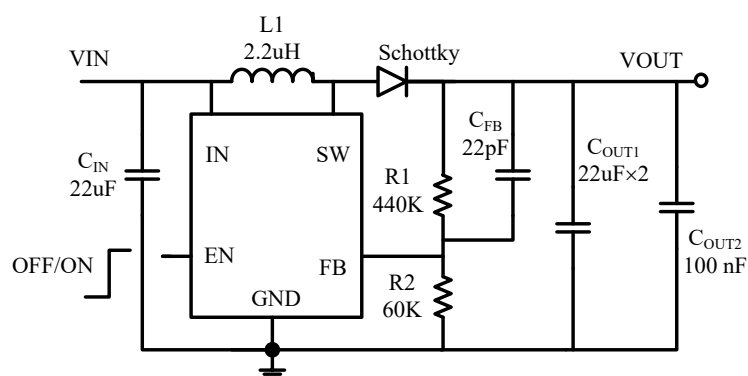

Fig 7 Vout Ripple

Fig 8 Quiescent Current Vs Temperature

■ **Typical Application Circuit**

Typical application

■ **Operation Description**

The J O ; 447D adopts fixed frequency, peak current mode boost regulator architecture to regulate output voltage. The operating principle of the J O ; 447D can be easily understood by referring to the functional block diagram. At the beginning of each oscillator cycle the MOSFET is turned on by the control circuit. To prevent sub-harmonic oscillations at duty cycle larger than 50 percent, a stabilizing ramp is added to the output of the current sense amplifier and the result is fed into the negative input of the PWM comparator. When this voltage equals the output voltage of the error amplifier, the power MOSFET is turned off. The voltage at the output of the error amplifier is an amplified result of the difference between the 0.6V reference voltage and the feedback voltage. In this way the peak current level keeps the output voltage in regulation. If the feedback voltage starts to drop, the output of the error amplifier increases, resulting in more current to flow through the power MOSFET, thus increasing the power delivered to the output. The J O ; 447D has internal soft start to avoid rush input current during the startup and also to avoid overshoot on the output.

■ **Application Information**

Because of the high integration in the J O ; 447D, the application circuit based on this regulator IC is rather simple. Only input capacitor C_{IN}, output capacitor C_{OUT1} and C_{OUT2}, inductor L, schottky diode and feedback resistors (R1 and R2) need to be selected for the targeted applications.

Feedback Resistor Divider R1 and R2:

Choose R1 and R2 to program the proper output voltage. To minimize the power consumption under light loads, it is desirable to choose large resistance values for both R1 and R2. A value of between 30KΩ and 500KΩ is recommended for both resistors. If R1=440KΩ is chosen and VOUT is 5V, then R2 can be calculated to be 60KΩ based on the following equation:

R2 = (R1×0.6V)/(VOUT - 0.6V)

Feedback Capacitor C_{FB}:

In order to enhance response speed of the convertor, feedback capacitor C_{FB} should be added to the loop. Its value should not be less than 22pF.

Input Capacitor C_{IN}:

To minimize the potential noise problem, place a typical X5R or better grade ceramic capacitor really close to the IN and GND pins. Care should be taken to minimize the loop area formed by CIN, and IN/GND pins. In this case a 10uF low ESR ceramic is recommended.

Output Capacitor C_{OUT1}And C_{OUT2}:

The output capacitor is selected to meet the output ripple noise requirements. Both steady state ripple and transient requirements must be taken into consideration when selecting this capacitor. For the best performance, it is recommended C_{OUT1} should be X5R or better grade ceramic capacitor with 10V rating and more than two pieces of 22uF Capacitor. Only when C_{OUT1} is big enough, it can absorb the energy of inductor and prevent the voltage of output up to too high when current load suddenly be shut. It is recommended C_{OUT2} is 100nF. It can also reduce the ripple of output voltage.

Boost Inductor L:

The recommended value of inductor is 1uH. Small size and better efficiency are the major concerns for portable devices. The inductor should have low core loss at 1.2MHz and low DCR for better efficiency. To avoid inductor saturation current rating should be considered.

Diode Selection:

Schottky diode is a good choice for J O ; 447D because of its low forward voltage drop and fast reverses recovery in order to get better efficiency. The high speed rectification is also a good characteristic of Schottky diode for high switching frequency. The diode reverse breakdown voltage should be larger than the output voltage, and its forward voltage should be less than 0.6V.

Start-up and Inrush Current:

The J O ; 447D has internal soft start to limit the value of current through VIN during the startup and also to avoid overshoot on the output. The soft start is realized by gradually increasing the output of error amplify during start-up.

Over Voltage Protection:

The J O ; 447D has been integrated over voltage protection function. If the output voltage exceeds the targeted value of 12%, the internal circuit will shut power MOS, until V_{OUT} voltage falls down.

Layout Guidelines

In order to maximize efficiency, switch rise and fall times are very fast. To prevent radiation of highfrequency noise (for example, EMI), proper layout of the high-frequency switching path is essential. Minimize thelength and area of all traces connected to the SW pin, and always use a ground plane under the switchingregulator to minimize interplanecoupling.The input capacitor needs to be close to the VIN pin and GND pin in order to reduce the ripple of VIN.

The layout should also be done with well consideration of the thermal as this is a high power density device. Athermal pad connected to GND internally improves the thermal capabilities of the package should be soldered to the large ground plate,usingthermalvias underneath the thermal pad.

■ **Ordering Information**

Part Number	OVP(V)	Package	Marking
J O ; 447D	Vout×112%	SOP8-EP	9225B XXXX

■ Package Outlines

SOP8-EP

DETAIL A

DETAIL A
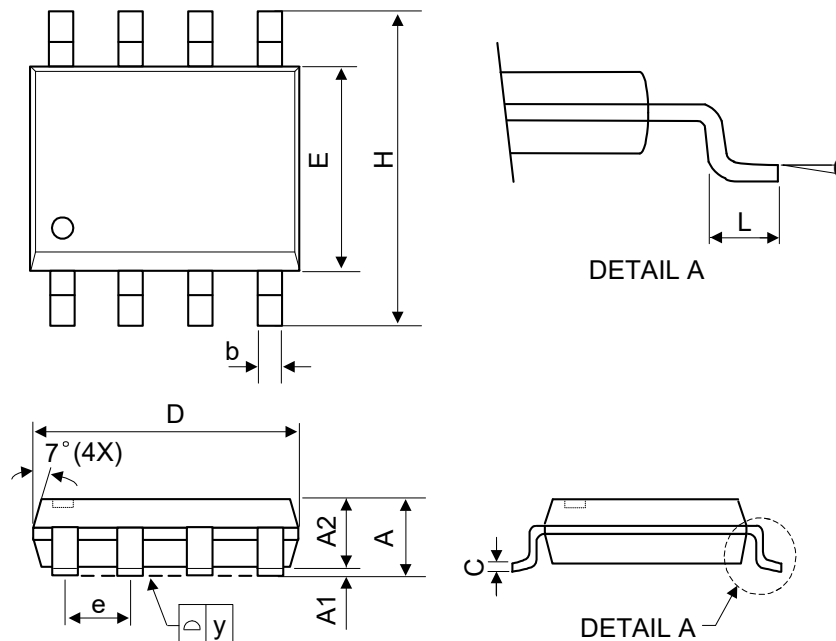
SYMBOL	MILLIMETER			INCHES		
	MIN	NOM	MAX	MIN	NOM	MAX
A	-	-	1.75	-	-	0.069
A1	0.1	-	0.25	0.04	-	0.1
A2	1.25	-	-	0.049	-	-
C	0.1	0.2	0.25	0.0075	0.008	0.01
D	4.7	4.9	5.1	0.185	0.193	0.2
E	3.7	3.9	4.1	0.146	0.154	0.161
H	5.8	6	6.2	0.228	0.236	0.244
L	0.4	-	1.27	0.015	-	0.05
b	0.31	0.41	0.51	0.012	0.016	0.02
e	1.27 BSC			0.050 BSC		
y	-	-	0.1	-	-	0.004
θ	0°	-	8°	0°	-	8°

■ **Packing Information**
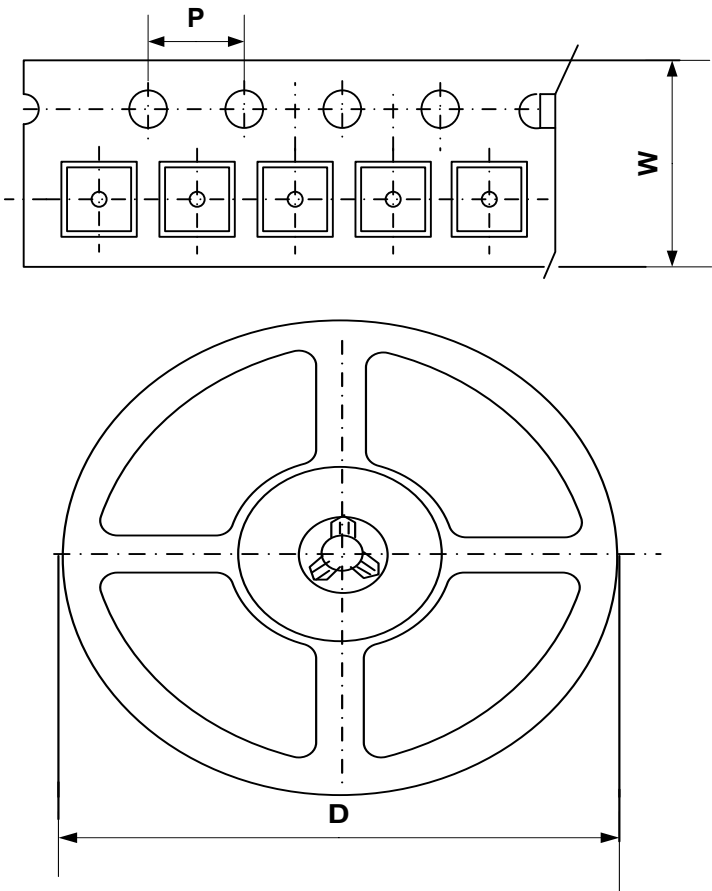
Package Type	Carrier Width (W)	Pitch (P)	Reel Size(D)	Packing Minimum
SOP8-EP	12.0±0.1 mm	8.0±0.1 mm	330±1 mm	2500pcs

Note: Carrier Tape Dimension, Reel Size and Packing Minimum