GENERAL DESCRIPTION

The HM6220 is an efficient linear voltage regulator with an ultralow-noise output, a very low dropout voltage (typically 17mV at light loads and 165mV at 150mA), and a very low ground current $(600\mu A \text{ at } 100\text{mA} \text{ output})$. The HM6220 offers better than 1% initial accuracy.

Designed especially for hand-held, battery-powered devices, the HM6220 includes a CMOS- or TTL-compatible enable/shutdown control input. When shut down, its power consumption drops nearly to zero. The regulator ground current increases only slightly in a dropout, further prolonging the battery life.

The HM6220 key features are a reference bypass (BYP) pin to improve its already excellent low-noise performance, reversed-battery protection, current limiting, and overtemperature shutdown. The HM6220 is available in fixed (-XX) and adjustable (Adj) output voltage versions in a small SOT-23-5 package.

The fixed output voltage version - HM6220-XX - may have a nominal output voltage (XX) within 1.5V to 12V.

FEATURES

- Ultralow-noise output
- High output voltage accuracy
- Guaranteed 150mA output
- Low quiescent current
- Low dropout voltage
- Extremely tight load and line regulation
- Very low temperature coefficient
- Current and thermal limiting
- Reverse-battery protection
- "Zero" off-mode current
- Logic-controlled electronic enable

APPLICATIONS

- Cellular telephones
- Laptop, notebook, and palmtop computers
- Battery-powered equipment
- PCMCIA V_{CC} and V_{PP} regulation/switching
- Consumer/personal electronics
- SMPS post-regulator/dc-to-dc modules
- High-efficiency linear power supplies

TYPICAL APPLICATION

J O 8442-XX

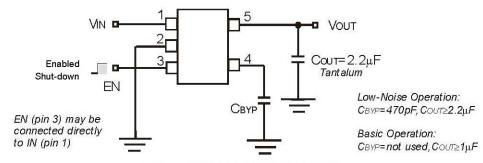


Fig.1. Ultralow-noise regulator

PIN CONFIGURATION

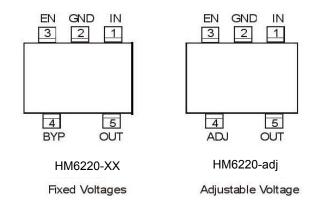


Fig.2

PIN DESCRIPTION

Pin		Name	Function	
HM6220-XX	HM6220-adj			
1	1	IN	Supply input	
2	2	GND	Ground	
3	3	EN	Enable/Shutdown input: CMOS-compatible. Logic High = Enabled. Logic Low or Open = Shut-down.	
4		BYP	Reference bypass: connect external 470pF capacitor to GND to reduce output noise. May be left open.	
	4	ADJ	Adjust input: adjustable regulator feedback input. Connect to resistor voltage divider	
5	5	OUT	Regulator output	

ABSOLUTE MAXIMUM RATINGS (Note 1)

Supply input voltage (V _{IN})	-20V to +20V
EN (enable) input voltage (V _{EN})	20V to +20V
Power dissipation (P _D)	Internally limited (Note 2)
Lead temperature (soldering, 5 sec.)	260°C
Junction temperature (T _J)	-40°C to +125°C
Storage temperature (T _{STG})	-65°C to +150°C

OPERATING RATINGS (Note 3)

Input voltage (V _{IN})	+2.0V to +16V
EN input voltage (V _{EN})	
Junction temperature (T _J)	40°C to +125°C
Thermal resistance, SOT-23-5 (θ ₁ Δ)(Note 2)



HD -)) ' 150mA LOW-NOISE LDO REGULATOR

ELECTRICAL CHARACTERISTICS

(at $V_{IN}=V_{OUT}+1V$, $I_L=100\mu A$, $C_L=1.0\mu F$, $V_{EN}\geq 2.0V$, $T_J=25^{\circ}C$, unless specified otherwise; the **bold** values indicate -40°C< T_J <+125°C)

Symbol	Parameters	Conditions	Min	Тур.	Max	Units
V _{OUT} (Note 4)	Output voltage accuracy	Variation from specified V _{OUT}	-1 -2		1 2	% %
ΔV _{Ουτ} /ΔΤ	Output voltage temperature coefficient	(Note 5)		40		ppm/°C
$\Delta V_{OUT}/V_{OUT}/V_{IN}$	Line regulation	V _{IN} = V _{OUT} +1V to 16V		0.004	0.012 0.05	%/V %/V
$\Delta V_{OUT}/V_{OUT}$	Load regulation	I _L =0.1mA to 150mA (Note 6)		0.02	0.2 0.5	% %
V _{IN} -V _{OUT}	Dropout voltage (Note 7)	I _L =100μA		10	50 70	mV mV
		I _L =50mA		110	150 230	mV mV
		I _L =100mA		140	250 300	mV mV
		I _L =150mA		165	275 350	mV mV
I _{GND}	Quiescent current	$V_{EN} \le 0.4V$ (shut-down) $V_{EN} \le 0.18V$ (shut-down)		0.01	1 5	μA μA
I_{GND}	GND pin current (Note 8)	V _{EN} ≥2.0V, I _L =100μA		120	160 180	μ Α μ Α
		I _L =50mA		350	600 800	μ Α μ Α
		I _L =100mA		600	1000 1500	μ Α μ Α
		I _L =150mA		1300	1900 2500	μ Α μ Α
PSRR	Ripple Rejection	frequency=100Hz, I _L =100μA		75		dB
I _{LIMIT}	Current limit	V _{OUT} =0V		320	600	mA
$\Delta V_0/\Delta P_D$	Thermal Regulation	(Note 9)		0.05		%/W
E _{no}	Output Noise	I_L =50mA, C_L =2.2μF, 470pF from BYP to GND		260		$\frac{nV}{\sqrt{Hz}}$
Enable input	_1	I				V 112,
V _{IL}	EN input logic Low voltage	Regulator shut-down			0.4 0.18	V V
V _{IH}	EN input logic High voltage	Regulator enabled	2.0			V
I _{IL}	EN input current	V _{IL} ≤0.4V		0.01	1	μА
		V _{IL} ≤0.18V			2	μА
I _{IH}	<u> </u>	V _{IH} ≥2.0V	2	5	35	μА
		V _{IH} ≥2.0V		1	40	μА

- Note 1: Exceeding the absolute maximum rating may damage the device.
- Note 2: The maximum allowable power dissipation at any T_A (ambient temperature) is $P_{D(max)} = (T_{J(max)} T_A) + \theta_{JA}$. Exceeding the maximum allowable power dissipation will result in excessive die temperature, and the regulator will go into thermal shutdown. The HM6220 (all versions) θ_{JA} value is 220°C/W (the chip is mounted on a PC board).
- Note 3: The device is not guaranteed to function outside its operating rating.
- Note 4: HM6220-adj has V_{REF} =1.242±1%, but the minimum output voltage for HM6220-adj must be above $V_{OUT(min)}$ = 1.5V
- Note 5: The **Output voltage temperature coefficient** is defined as the worst case voltage change divided by the total temperature range.
- Note 6: The **Load regulation** is measured at a constant junction temperature using low duty cycle pulse testing. The parts per this parameter are tested in the load range of 0.1mA to 150mA.
- Note 7: The **Dropout voltage** is defined as the input-to-output differential, at which the output voltage drops 2% below its nominal value measured at 1V differential. At very low values of programmed output voltage, the minimum input supply voltage of 2 V must be taken into account.
- Note 8: The **GND** pin current is the regulator Quiescent current plus the pass transistor base current. The total current drawn from the supply is the sum of the load current plus the GND pin current.

Note 9. Thermal regulation is defined as the change in output voltage at a time "t" after a change in power dissipation is applied, excluding load or line regulation effects. Specifications are for a 150mA load pulse at V_{IN} = 16V for t = 10ms

BLOCK DIAGRAMS

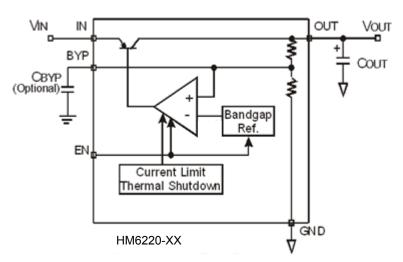


Fig.3a. Ultralow-noise fixed regulator

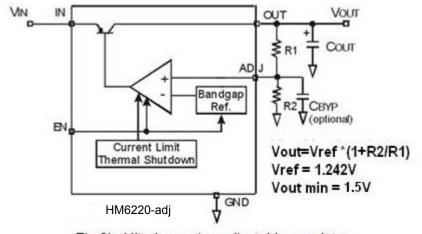


Fig.3b. Ultralow-noise adjustable regulator

